

SiPROM OTP Memory

Product Brief

Sidense OTP memory IP is based on a patented, area-efficient antifuse cell – **1T-Fuse™** – employing gate oxide breakdown as a programming mechanism. Available in a standard CMOS process, Sidense macrocells do not require any additional mask layers or process steps and provide an alternative to mask ROM, eFuses and Flash memory in many applications.

The reduced size of the single transistor bit-cell results in better yield, higher security, improved reliability and lower overall product cost.

SiPROM OTP

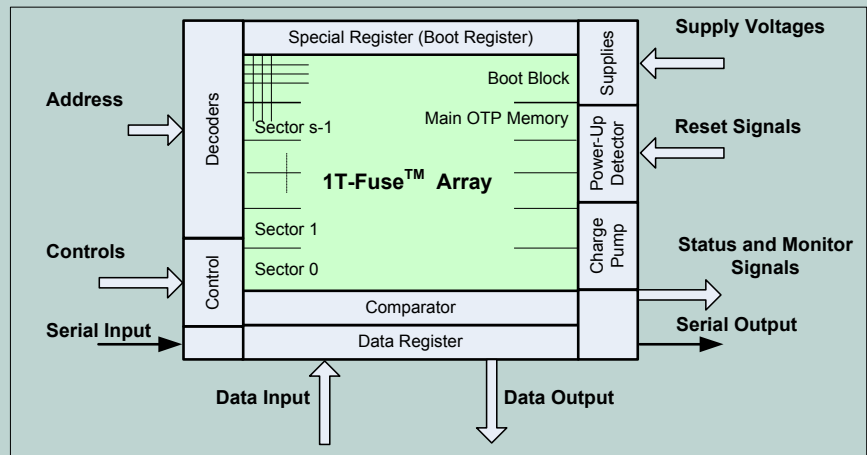
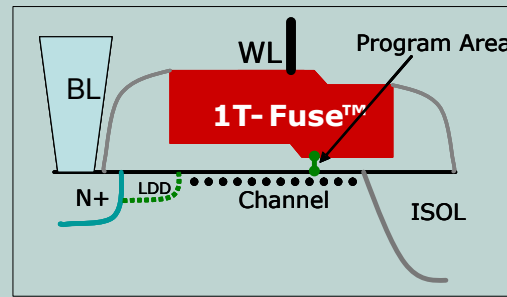
- Retention exceeding 20 years constant read at T_{max}
- Standard CMOS process
- Available from 130nm to 40nm
- Highly secure
- Fast read access
- Multiple read modes
- Flexible Mask ROM option
- Optional Serial Test Port

Applications

- HDCP encryption key
- Mobile and wireless
- Analog trim and calibration
- Boot code and firmware storage
- Medical
- Automotive
- Chip ID
- Emulated MTP

Deliverables

- Datasheets
- Application notes
- Verilog model
- Test bench
- LIB
- LEF
- LVS netlist
- GDSII



The SiPROM memory is silicon proven and available in several different configurations with sizes up to 512 Kbits per macro, using multiple macros for higher memory capacity.

All SiPROM macrocells include the following features:

- Integrated charge pump for field programming
- Row redundancy for defective cell/row repair
- Differential and 100% Redundant read modes
- Hierarchical Bank/Block/Sector organization
- Boot Block and a Special Boot Register for macrocell access control

The Sidense SiPROM macrocell includes several additional features that can be utilized to give the user more flexibility in customizing the memory operation to target a specific application.

Built-in Charge Pump

The embedded charge pump allows the customer to program the SiPROM macrocell in the field after the SoC is packaged, eliminating the need for additional power supplies to the SoC.

Row Redundancy

All SiPROM macrocells integrate a row repair mechanism. Once set up, any defect repairs are transparent to the application.

Boot Row Register

The boot row register provides the user with an additional set of parallel outputs and can be used to control security locks, macrocell access, emulated multiple-time programmability, or any other customer defined options that need to be available immediately after power-up or reset.

Security Locks

This feature allows the user to disable the programming of the macrocell or a sector in the macrocell. In a typical application, the security lock pins are directly connected to the boot register pins and can lock programming access through macrocell power-up.

Mask ROM Option

The Sidense SiPROM macros can be converted into mask-programmable ROMs with a single mask change. The user has the flexibility to mask program the entire memory or individual portions of the macrocell.

This feature gives the customer the ability to mask program a section of the memory while allowing other sections of the memory to be programmed in the field.

About Sidense Corp.

Sidense Corp., founded in 2004, is a leading provider of secure, very dense and reliable non-volatile, one-time programmable (OTP) memory IP. Based on the Company's patented 1T-Fuse™ one-transistor bit cell, Sidense OTP is implemented in standard-logic CMOS processes with no additional masks or process steps required. Sidense OTP is available from 180nm to 28nm.

The information in this document is current as of its date of publication. Specifications are subject to change without notice.

SiPROM Features

- Standard CMOS Logic Process
- Up to 512 Kbits per macro (multiple macros can be used for higher memory capacity)
- Up to 128 IO bits per macrocell
- Multiple banks programmable in parallel
- Built-in charge pump for in-field programming
- Built-in row redundancy
- Built-in OTP Boot Block
- Special Boot Register for Power-up configuration
- Built-in power-up detector
- Incremental in-field programming
- Sector lock function
- Serial and/or parallel access
- Read access as low as 10ns
- Low read power consumption
- Power down mode
- Built-in Comparators for program verify
- Built-in Test Modes

To obtain more details about the SiPROM OTP family or other Sidense products, please contact:

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