

# ULP OTP Memory

## Product Brief

### ULP OTP

- Standard CMOS Logic Process
- Highly secure
- Ultra low power consumption
- Multiple read modes
- Flexible Mask ROM option

### Applications

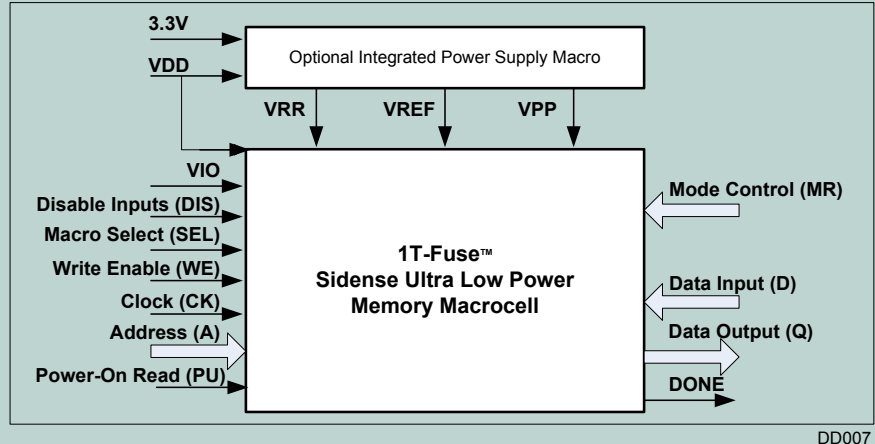
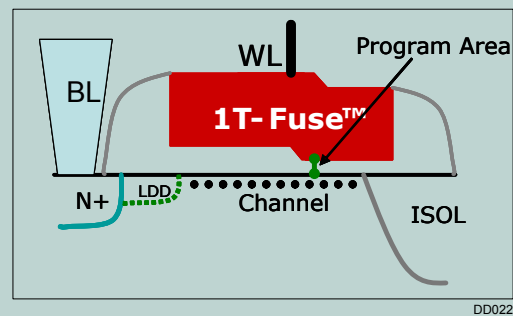
- HDCP encryption key
- Mobile and wireless
- Analog trim and calibration
- Boot code and firmware storage
- Medical
- Automotive
- Chip ID
- RFID
- Emulated MTP

### Deliverables

- Datasheets
- Application notes
- Verilog model
- Test bench
- LIB
- LEF
- LVS netlist
- GDSII

Sidense OTP memory IP is based on a patented, area-efficient antifuse **1T-Fuse™** cell employing gate oxide breakdown as a programming mechanism. Available in a standard CMOS process, Sidense macrocells do not require any additional mask layers or process steps.

The reduced size of the single transistor bit-cell results in better yield, higher security, improved reliability and lower overall product cost.



The ULP macrocell is designed to minimize active and standby power consumption. The macrocell integrates three read operating modes (Single-ended, Differential and Redundant), and several test modes to simplify production testing and programming verification.

The Sidense ULP macrocell includes several additional features which can be utilized to give the user more flexibility in customizing the memory operation to target a specific application.

## Read Mode Options

By default, the OTP macrocells are read in differential-redundant mode utilizing four memory cells per logical bit of information at a low VDD level. The ULP macrocell can also be read in single-ended mode utilizing one memory cell per logical bit of information at a standard VDD level.

## Special Operating and Test Modes

The ULP macrocell has special operating and test modes, such as sense amplifier test mode, wordline test mode and bitline test mode that can be enabled in order to reliably test the macrocell. Unlike most OTP, testing can be achieved on both the programmed and the un-programmed cells.

## Mask ROM Option

The Sidense ULP macros can be converted into mask programmable ROMs with a single layer change. The user has the flexibility to mask program the entire memory or individual portions of the macrocell.

This feature gives the customer flexibility to mask program a section of the memory while allowing other sections of the memory to be programmed in the field.

## Optional Integrated Power Supply Macro

The Sidense ULP macros can be combined with the Sidense IPS (Integrated Power Supply) to allow the customer to program the ULP macrocell in the field after the SOC is packaged, eliminating the need for additional power supplies to the SOC.

## About Sidense Corp.

Sidense Corp., founded in 2004, is a leading provider of secure, very dense and reliable non-volatile, one-time programmable (OTP) memory IP. Based on the Company's patented 1T-Fuse™ one-transistor bit cell, Sidense OTP is implemented in standard-logic CMOS processes with no additional masks or process steps required. Sidense OTP is available from 180nm to 28nm.

## ULP Features

- Standard CMOS Logic Process  
1.8V core, 3.3V IO voltage
- Up to 2Kbits per macrocell
- Multiple macrocells can be combined for larger OTP sizes
- Up to 128 IO bits per macrocell
- Optional Integrated Power Supply (IPS)
- Ultra low read power consumption
- Power-On Read function
- Built-in word-line test mode
- Built-in bit-line test mode
- Built-in sense amplifier test mode
- Built-in cell margin modes for programming verification

To obtain more details about the ULP OTP product family or other Sidense products, please contact:

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